WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a floating gate electrode;

a first source/drain region having a diode structure employed for controlling the potential of said floating gate electrode; and

a second source/drain region formed to hold a channel region between said first source/drain region and said second source/drain region.

sub A1 2. The semiconductor memory according to claim 1, wherein

a negative voltage is applied to said first source/drain region having a diode structure in erasing.

3. The semiconductor memory according to claim 1, wherein

said first source/drain region includes:

a second conductivity type first impurity region (4a) formed on a first layer consisting of a first conductivity type semiconductor, and

a first conductivity type second impurity region (4b, 4c) formed inside said first impurity region, and

said first impurity region is formed on the overall

region between said first layer and said second impurity region.

4. The semiconductor memory according to claim 3, wherein

said second impurity region includes: (4b or/and 4c)

a first conductivity type third impurity region (4b) formed on said first layer to be in contact with said first impurity region (4a), and

a fourth impurity region (4c) formed by a first conductivity type semiconductor film embedded in said third impurity region.

5. The semiconductor memory according to claim 1, wherein

said second impurity region is capacitively coupled with said floating gate electrode through a first insulator film.

6. The semiconductor memory according to claim 5, further comprising:

a control gate electrode formed on said channel region through a gate insulator film,

a semiconductor region formed between said control gate electrode and said floating gate electrode,

a first tunnel insulator film formed between said semiconductor region and said control gate electrode, and

a second tunnel insulator film formed between said semiconductor region and said floating gate electrode,

for writing data by injecting hot carriers into said floating gate electrode from said control gate electrode through said first tunnel insulator film, said semiconductor region and said second tunnel insulator film.

7. The semiconductor memory according to claim 6, wherein

the area of said first insulator film located between said second impurity region and said floating gate electrode is larger than the area of said second tunnel insulator film located between said semiconductor region and said floating gate electrode.

8. The semiconductor memory according to claim 7, wherein

a voltage applied to said second impurity region is transmitted to said floating gate electrode through electrostatic coupling between said second impurity region and said floating gate electrode so that a transistor having said floating gate electrode as the gate enters an ON state and the potential of said semiconductor region

reaches a level substantially identical to the potential of said second impurity region.

9. The semiconductor memory according to claim 6, wherein

said semiconductor region has a second conductivity type.

10. The semiconductor memory according to claim 6, wherein

the width of said semiconductor region is set substantially not more than the mean free path of carriers, transmitted through the barrier of said first tunnel insulator film between said control gate electrode and said semiconductor region, having energy necessary for tunneling through the barrier of said second tunnel insulator film.

11. The semiconductor memory according to claim 5, further comprising:

a control gate electrode formed on said channel region through a gate insulator film, and

a tunnel insulator film formed between said control gate electrode and said floating gate electrode,

for writing data by injecting hot carriers from said

channel region into said floating gate electrode.

12. The semiconductor memory according to claim 1, further comprising:

a control gate electrode formed on said channel region through a gate insulator film, and

a tunnel insulator film formed between said control gate electrode and said floating gate electrode, wherein

the thickness of said gate insulator film located under said control gate electrode is smaller than the thickness of said tunnel insulator film located between said control gate electrode and said floating gate electrode.

13. The semiconductor memory according to claim 12, wherein

the thickness of said gate insulator film located under said control gate electrode is not more than half the thickness of said tunnel insulator film located between said control gate electrode and said floating gate electrode.

14. A semiconductor device comprising:

a first source/drain region and a second source/drain region formed on a first layer consisting of a first

conductivity type semiconductor to hold a channel region therebetween; and

a gate electrode formed on said channel region, wherein

either said first source/drain region or said second source/drain region has a diode structure.

15. The semiconductor device according to claim 14, wherein

said first or second source/drain region having a diode structure includes:

a second conductivity type first impurity region formed on said first layer consisting of said first conductivity type semiconductor, and

a first conductivity type second impurity region formed inside said first impurity region, and

said first impurity region is formed on the overall region between said first layer and said second impurity region.